

deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would result in deadlock if a predetermined further transaction were to begin, this condition is detected. In the more tightly coupled system, the predetermined further transaction is refused if requested, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transaction is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.]

IN THE SPECIFICATION

Replace the paragraph at column 1, line 4, with the following paragraph:

Notice: More than one reissue application has been filed for the reissue of Patent No. 5,996,036. The reissue applications are application numbers 10/669,119 (the present application), and 10/006,939. This application is a continuation of application 10/006,939, which is a continuation-in-part of U.S. Patent Application No. 08/432,622, filed May 2, 1995, now abandoned.